

REMARKS

Claims 1 and 2 have been amended. Claim 9 has been added. Claims 1-4 and 9 are pending. Figure 9 has been amended. A supplemental declaration is attached.

Oath or Declaration

The Applicants have attached a supplemental declaration in accordance with 37 C.F.R. 1.67(a).

However, the Applicants assert that the previously submitted declaration is in compliance with 37 C.F.R. 1.63, MPEP 602 and, in particular, 605.03. "The mailing or post office address should include the ZIP Code designation" (emphasis added). MPEP 605.03. The language "should" is directory and not obligatory. Also, a ZIP Code (a registered TM from an acronym for "Zoning Improvement Plan") is part of United States practice used by the U.S. Postal Service. The term "ZIP Code" has no meaning, force or effect in the Japan postal service.

The supplemental declaration includes a Japan postal zone as a substitute for the ZIP Code.

Specification

The title of the specification has been replaced by, "Semiconductor Device with Reduced Local Current Crowding," as required by the Examiner.

Drawings

Figure 9 on drawing sheet 5 has been amended to include the legend "Prior Art." A replacement drawing sheet is attached hereto.

Claim Rejections – 35 U.S.C. 102

Claims 1-4 were rejected in the Office action as being anticipated by U.S. Patent No. 6,255,154 to Akaishi et al.

Claim 1 has been amended to recite, “the first gate insulating film does not extend lower than the second gate insulating film.” The amendment clarifies the relationship between the first and second gate insulating films. As shown, for example, in the particular embodiment of Fig. 8, the lowest that the second gate insulating film (7) extends is as far as the first gate insulating film (8). Both of the gate insulating films are not lower than the upper surface of the semiconductor substrate (1). *See, for example*, page 5 line 6-8 and FIG 8.

In contrast, Akaishi et al. discloses a second gate insulating film (9) that extends below the first gate insulating film (6). The second gate insulating film (9) extends below the upper surface of the semiconductor substrate (1). *See* FIG 11B. Akaishi et al. only shows the prior art structure illustrated in FIG. 9 of the present application, which also shows the second gate insulating film (56) below the first gate insulating film (57).

Akiashi et al. does not teach or suggest having a structure with the first gate insulating film not extending lower than the second gate insulating film as recited in claim 1. Akaishi et al. also does not recognize that the structure recited in claim 1 can reduce local current crowding in such a manner that a concave/convex region at a boundary surface between the semiconductor substrate (1) and the gate insulating films (6, 7) is eliminated so as to distribute equipotential lines.

In view of the amendment and the above remarks, the Applicants respectfully request withdrawal of the 35 U.S.C. 102 rejection of claim 1.

Claims 2-4 depend from claim 1 and should be allowable for at least the same reasons.

Miscellaneous

Claim 2 has been amended to correct a syntactical error in verb and object agreement.

Conclusion

Applicants respectfully request allowance of all pending claims.

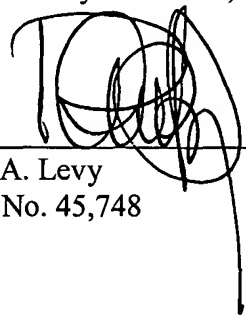
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Enclosed is a \$110 check for the Petition for Extension of Time fee. Please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,

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